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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,606	03/31/2004	Richard A. Johnson	SIL.00006US	5455
21906	7590	06/09/2008	EXAMINER	
TROP PRUNER & HU, PC 1616 S. VOSS ROAD, SUITE 750 HOUSTON, TX 77057-2631			LE, NHAN T	
ART UNIT	PAPER NUMBER			
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/814,606	<b>Applicant(s)</b> JOHNSON, RICHARD A.
	<b>Examiner</b> NHAN T. LE	<b>Art Unit</b> 2618

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 18 February 2008.  
 2a) This action is FINAL.      2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-34 and 49-57 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) 10-34 is/are allowed.  
 6) Claim(s) 1 and 49-56 is/are rejected.  
 7) Claim(s) 2-9 and 57 is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)            | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claim 1, 49-53, 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gurvich et al (US 20030042979) in view of Leffel (US 6,255,903).

As to claim 1, Gurvich teaches a magnetically differential input circuit to couple a single-ended signal source to a single-ended receiving circuit (see fig. 2, paragraphs 0033-0036) the input circuit comprising: a first terminal (see fig. 2, number 100, paragraphs 0033-0036) to couple to an output of the single-ended signal source; a second terminal (see fig. 2, number 107, paragraphs 0033-0036) to couple to a signal return; a third terminal (see fig. 2, number 103, paragraphs 0033-0036); a first loop (see fig. 2, first loop, paragraphs 0033-0036) comprising the first terminal and the second terminal; and a second loop (see fig. 2, second loop, paragraphs 0033-0036) comprising the second terminal and the third terminal. Gurvich fails to teach wherein a second terminal coupled to the signal ground, a third terminal to couple to an output of the single-ended signal source. Leffel teaches wherein a second terminal coupled to switch and a third terminal to couple to an output of the single-ended signal source (see fig. 1, numbers 20, 134, col. 2, line 38-65, col. 3, lines 1-59). Therefore, it would have

been obvious to one of ordinary skill in the art at the time the invention was made to provide the teaching of Leffel into the system of Gurvich in order to improve the linearity of the amplifier.

As to claim 49, Gurvich teaches an input circuit comprising: a first loop including a first terminal to receive a signal from a signal source and a second terminal to couple to a signal ground (see fig. 2, first loop, paragraphs 0033-0036); and a second loop including a third terminal to receive the signal from the signal and the second terminal (see fig. 2, first loop, paragraphs 0033-0036). Gurvich fails to teach wherein the first and second loops are arranged so that a first interfering signal induced in the first loop by an interference source is cancelled by a second interfering signal induced in the second loop by an interference source. Leffel teaches wherein the first and second loops are arranged so that a first interfering signal induced in the first loop by an interference source is cancelled by a second interfering signal induced in the second loop by an interference source (see col. 2, line 38-65, col. 3, lines 1-59). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teaching of Leffel into the system of Gurvich in order to improve the linearity of the amplifier.

As to claim 50, the combination of Gurvich and Leffel teaches wherein the first loop physically matches the second loop (see Gurvich fig. 2, first loop, second loop, paragraphs 0033-0036).

As to claim 51, the combination of Gurvich and Leffel teaches wherein the first and second loops circumscribe substantially equal areas (see fig. 2, first loop, second

loop, paragraphs 0033-0036).

As to claim 52, the combination of Gurvich and Leffel teaches wherein the first, second and third terminals are substantially collinear and the second terminal is disposed intermediate between, and substantially equidistant from, the first terminal and the third terminal (see Gurvich fig. 2, number 107, paragraphs 0033-0036).

As to claim 53, the combination of Gurvich and Leffel teaches wherein the first and second loops effect cancellation of an induced interfering voltage at a receiving circuit coupled to the input circuit (see Gurvich fig. 2, second loop, paragraphs 0033-0036).

As to claim 56, the combination of Gurvich and Leffel teaches wherein the first and second loops traverse an input of the transceiver in opposite directions (see Gurvich fig. 2, first loop, second loop, paragraphs 0033-0036).

2. Claims 54, 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gurvich et al (US 20030042979) in view of Leffel (US 6,255,903) further in view of Schwarzmueller (US 7,120,217).

As to claim 54, the combination of Gurvich and Leffel teaches the first, second and third terminals. Gurvich fails to teach wherein the first, second and third terminals comprise pins on an integrated circuit package, the integrated circuit package including a transceiver. Schwarzmueller teaches wherein different circuit components on IC (see col. 5, lines 66-67, col. 6, lines 1-18). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teaching of

Schwarzmueller into the system of Gurvich and Leffel in order to provide the small and less interference circuit.

As to claim 55, the combination of Gurvich, Leffel and Schwarzmueller teaches wherein the first and third terminals are diametrically opposite and mutually adjacent to the second terminal (see Gurvich fig. 2, numbers 100, 107, 103, paragraphs 0033-0036).

***Allowable Subject Matter***

3. Claims 2-9, 57 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As to claim 2, the applied reference fails to teach wherein the first loop and the second loop circumscribe substantially equal areas and are arranged so that a first interfering signal induced in the first loop by a source of interference is cancelled by a second interfering signal induced in the second loop by the source of interference as cited in the claim.

As to claim 7, the applied reference fails to teach wherein the first, second and third terminals are substantially collinearly juxtaposed and the second terminal is disposed intermediate between, and substantially equidistant from, the first terminal and the third terminal as cited in the claim.

As to claim 57, the applied reference fails to teach comprising a third loop within the integrated circuit package, wherein the first interfering signal induced in the first loop

by the third loop is to cancel the second interfering signal induced in the second loop by the third loop as cited in the claim.

4. Claims 10-34 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding Claim 10, Posner et al (US 20030064738) teaches spurious radio control circuit for use with feed-forward linear amplifier; Leffel (US 6,255,903) teaches linear power amplifier with configurable feed-forward error correction circuit; Gurvich et al (US 20030199257) teaches spurious radio control circuit for use with feed-forward linear amplifier. The teaching of these prior arts either combined or alone fails to teach a first conductor coupled to the first terminal and the input node; a second conductor coupled to the first terminal and the input node, wherein the terminals, circuit nodes and conductors are arranged to form a first loop and a second loop that effect cancellation of an induced interfering voltage at the receiving circuit.

Dependent claims 11-22 are allowable for the same reason.

Regarding Claim 23, Posner et al (US 20030064738) teaches spurious radio control circuit for use with feed-forward linear amplifier; Leffel (US 6,255,903) teaches linear power amplifier with configurable feed-forward error correction circuit; Gurvich et al (US 20030199257) teaches spurious radio control circuit for use with feed-forward linear amplifier. The teaching of these prior arts either combined or alone fails to teach a fourth terminal coupled to the second input node, wherein the first terminal and the

fourth terminal are included in a first loop and wherein the second terminal and the third terminal are included in a second loop that opposes the first loop.

Dependent claims 24-34 are allowable for the same reason.

***Response to Arguments***

5. Applicant's arguments with respect to claims 1-34, 49-57 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Le whose telephone number is 571-272-7892. The examiner can normally be reached on 08:00-05:00 (Mon-Fri).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on 571-272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Nhan T Le/  
Patent Examiner  
Art Unit 2618  
Nhan T. Le